| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/761,322 | HIRANO ET AL. | |
| | Examiner | Art Unit | |
| | Natalia Figueroa | 2651 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment (01 November 2005)*.

2. ☒ The allowed claim(s) is/are *2-16*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## REASONS FOR ALLOWANCE

### *Allowable Subject Matter*

1. Claims 2-16 are allowed.

2. The following is an examiner's statement of reasons for allowance:

RE claim 2, the prior art of record, and in particular "Correction Methods for Errors in Partial Response Channels", fails to teach or suggest a bit converting circuit for inputting an output of said coding device and bit converting a coded bit stream of a coded word with a parity; and a precoder for inputting an output of said bit converting circuit, and performing precoding according to 1/(1+D) as a delay operator, wherein said bit converting circuit performs bit conversion with a bit stream containing the parity bit.

RE claim 3, the prior art of record, and in particular "Correction Methods for Errors in Partial Response Channels", fails to teach or suggest a bit converting circuit for inputting an output of said coding device and bit converting a coded bit stream of a coded word with a parity; and a precoder for inputting an output of said bit converting circuit, and performing precoding according to 1/(1+D) as a delay operator, wherein said bit converting circuit performs bit conversion with a bit stream containing the parity bit., and wherein, when performing the bit conversion with the bit stream containing the parity bit, said coding device performs either conversion of bit patterns "*01-1-110", "011-1-10*" and "'011-1-110" (* is don't care) with the parity bit being "0", or conversion of a bit pattern "011-1-10" with the parity being "0", where a bit stream of a coded word of 3 bits immediately before the parity bit, one bit of the parity bit, and a bit stream of a coded word of 3 bits immediately after the parity bit are separated by a symbol"-".

RE claim 6, the prior art of record, and in particular "Correction Methods for Errors in Partial Response Channels", fails to teach or suggest a bit converting circuit for inputting an output of said parity generating circuit and bit converting a bit stream of a coded word to which a parity bit is added; a precoder for inputting an output of said converting circuit and performing precoding according to 1/(1+D) as a delay operator; wherein said recording is performed in such a manner that a value of a parity bit resulting from parity calculation of a bit stream as a target of the panty bit among bit streams recorded on said information recording medium does not necessarily coincide with a value of a parity bit recorded on said information recording medium correspondingly to the bit stream recorded on said information recording medium.

RE claim 7, the prior art of record, and in particular "Correction Methods for Errors in Partial Response Channels", fails to teach or suggest a bit converting circuit for inputting an output of said parity generating circuit and bit converting a bit stream of a coded word to which a parity bit is added; a precoder for inputting an output of said converting circuit and performing precoding according to 1/(1+D) as a delay operator; wherein said recording is performed in such a manner that a value of a parity bit resulting from parity calculation of a bit stream as a target of the parity bit among bit streams recorded on said information recording medium does not necessarily coincide with a value of a parity bit recorded on said information recording medium correspondingly to the bit stream recorded on said information recording medium, and wherein said recording is performed in a such a manner that a value of the parity bit is always "0", where a value of a parity bit resulting from parity calculation of a bit stream as a target of the parity bit among bit streams recorded on said information recording medium does not coincide with a

value of a parity bit recorded on said information recording medium correspondingly to the bit stream recorded on said information recording medium.

RE claim 8, the prior art of record, and in particular "Correction Methods for Errors in Partial Response Channels", fails to teach or suggest a bit converting circuit for inputting an output of said parity generating circuit and bit converting a bit stream of a coded word to which a parity bit is added; a precoder for inputting an output of said converting circuit and performing precoding according to 1/(1+D) as a delay operator; wherein said recording is performed in such a manner that a value of a parity bit resulting from parity calculation of a bit stream as a target of the parity bit among bit streams recorded on said information recording medium does not necessarily coincide with a value of a parity bit recorded on said information recording medium correspondingly to the bit stream recorded on said information recording medium, and wherein said recording is performed in a such a manner that a value of the parity bit is always "0", where a value of a parity bit resulting from parity calculation of a bit stream as a target of the parity bit among bit streams recorded on said information recording medium does not coincide with a value of a parity bit recorded on said information recording medium correspondingly to the bit stream recorded on said information recording medium, and wherein data recorded on said information recording medium has a continuous number "r" not larger than 3 or 4 of reverse times of record state of recorded information.

RE claims 9 and 12, the prior art of record, and in particular "Correction Methods for Errors in Partial Response Channels", fails to teach or suggest a Viterbi decoding circuit performs data discrimination by excluding from search candidates a transition path corresponding to a coded word series "1111"' in a process of searching a most likelihood path

corresponding to a case where the l's continuous number "'r" is 3, or by excluding from search candidates a transition path corresponding to a coded word series "11111" in a process of searching a most likelihood path corresponding to a case where the l's continuous number "r" is 4, or by excluding from search candidates transition path: corresponding to coded word series "11111", "001111" and "111100", in a process of searching a most likelihood path corresponding to a case where the l's continuous number "r" is 4; and said decoder includes a bit reverse-converting circuit and an error correction circuit, in which said bit reverse-converting circuit performs reverse-conversion of discriminated bit stream in a case of a bit stream of either "****-0-1110" or "0111-0-****" (* is don't care), where a bit stream of a coded word of 4 bits immediately before the parity bit, one bit of the parity bit, and a bit stream of a coded word of 4 bits immediately after the parity bit are separated by a symbol "-", and said error correction circuit corrects discrimination errors of 1 bit and 3 bits.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Natalia Figueroa whose telephone number is (571) 272-7554. The examiner can normally be reached on Monday - Thursday 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David R. Hudspeth can be reached on (571) 272-7843. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NFM

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